Design Handbook

*a*MEMS™ Process Technology

A RSC MEMS Technology

Rockwell Scientific Company, LLC

Revision 1.0

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*a*MEMS™ process technology is one of Rockwell Scientific's MEMS fabrication processes. The offering of the *a*MEMS™ process technology for external user access, including this Design Handbook, is supported in part by the Defense Advanced Research Projects Agency (DARPA) under DARPA/MTO BAA 04-10 MEMS Exchange program, titled "*a*MEMS Process Module for Versatile MEMS Implementation," contract number NBCHC040116.

Table of Contents

Section 1

*a*MEMS™ Process Technology Overview

1.1. Introduction

The *a*MEMS™ process technology is a highly versatile Silicon-on-Insulator (SOI) based fabrication process involving adhesive transfer bonding of the single crystal silicon device layer to a receiving substrate wafer. This process offers unique levels of process customization and device utility. The suitability for wide-reaching applications has been demonstrated through implementation of a broad spectrum of MEMS devices in the *a*MEMS process, including RF tunable capacitors, lateral contact switches, industrial process sensors, and inertial sensors [1-7]. The objective of the offering of the *a*MEMS™ process technology for external user access is to greatly facilitate rapid-turn device development among MEMS developers in industry and academia, while providing unparalleled process flexibility for exploring creative device concepts. Key highlights of the *a*MEMS™ process technology include:

- **Single crystal silicon** device structures, utilizing the well-established performance benefits of Si Deep Reactive Ion Etch (DRIE) processing with high dimensional tolerances;
- **Multiple substrate material selections** (e.g., silicon, high-? silicon, or glass), offering design flexibilities in, for example, reducing substrate parasitics in RF device structures, tailoring CTE difference with the Si device layer, or integrating electronics (in a customized run) onto the substrate wafer;

- Compatibility with **dielectric structural layers** – the ability to combine both single crystal Si and dielectric thin films as structural elements enables unique levels of electrical isolation (up to 1kV demonstrated) to be incorporated into device structures;
- **Low process temperature** budget of 200 ºC;
- Simple 2-mask level processing enables **rapid turn** from CAD acceptance to parts delivery;
- Highly **generic process** suitable to many different MEMS applications;
- Extreme **process flexibility** – *a*MEMS enables independent processing of both sides of the single crystal silicon device layer as well as the interior substrate surface, permitting unique device configurations unachievable through conventional SOI processing. This feature can be used (in a customized run) to exploit two-sided coatings for stress compensation or to integrate conductive coatings for reduced electrical resistance.

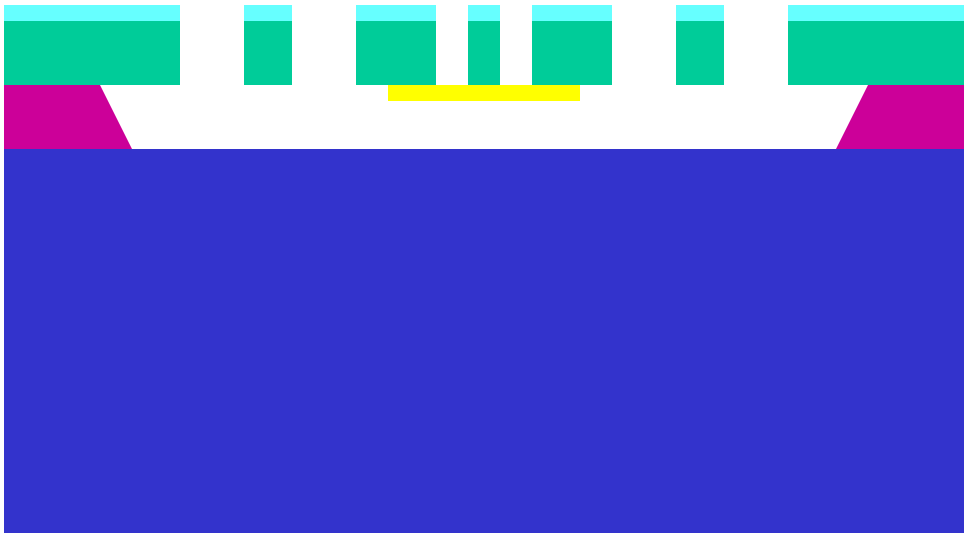


Figure 1.1. A cross sectional illustration of an exemplary *a*MEMS™ structure shows all layers of the baseline process (not to scale).

The *a*MEMS™ baseline process offers the following generic features with all layers shown in Fig. 1.1:

1. The primary structural material is a single crystal silicon layer from an SOI wafer with nominally a thickness of 20 µm and a resistivity of 0.1 O•cm.
2. A layer of evaporated aluminum with a nominal thickness of 0.5 µm is on top of the patterned silicon structural layer.
3. A layer of silicon dioxide film with a nominal thickness of 1.6 µm is independently patterned and beneath the silicon structural layer.
4. A substrate of choice is selected, (e.g., silicon or glass), with a nominal thickness of 500 µm.
5. An adhesive layer with a nominal thickness of 20 µm bonds the structural layers and the selected substrate.

1.2. Process Flow

The baseline *a*MEMS™ process technology is a 2-mask level SOI patterning and etching micromachining process, offering single crystal silicon MEMS device structural material and releasable silicon dioxide insulators that mechanically connect and electrically isolate adjacent silicon features. Also offered within the baseline 2-mask level *a*MEMS™ process technology are the necessary metallization and electrical isolations, providing a complete micromachining process for MEMS device prototyping and proof-of-concept demonstration.

The process begins with a 100-mm SOI wafer, as illustrated in Fig. 1.2, consisting of a silicon device layer nominally 20 µm (± 1 µm) thick. Both the silicon substrate material and the silicon dioxide Buried Oxide (BOX) layer of the starting SOI wafer are subsequently removed entirely as will be seen later in the process flow. The silicon device layer has a (100) crystal graphic orientation and a p-type resistivity between 0.01 O•cm and 10 O•cm, and serves as the primary structural material. A bottom side oxide layer, not shown in Fig. 1.2, may also be present on the bottom side of the SOI wafer.

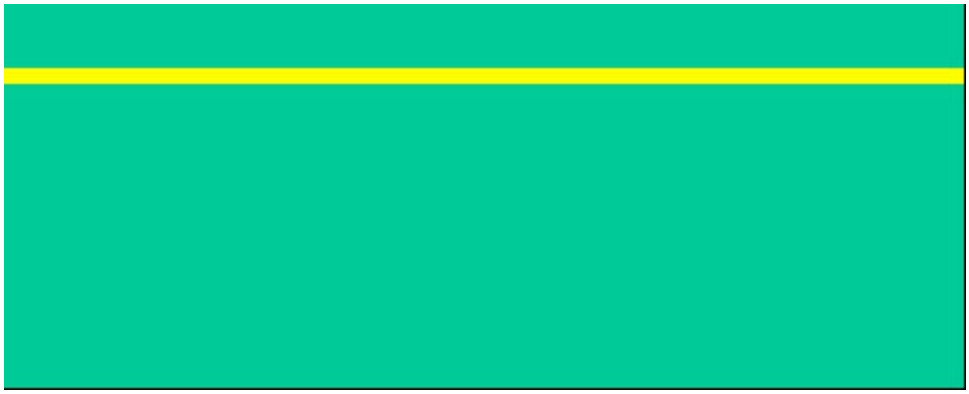


Figure 1.2. The starting material is a SOI wafer with a 20 µm silicon device layer, a 0.5 µm silicon dioxide layer, and a 500 µm silicon substrate layer.

Figure 1.3. A layer of PECVD silicon dioxide is deposited on top of the silicon device layer at a temperature of 200 ºC. The PECVD silicon dioxide layer serves subsequently as a releasable insulator structural layer.

A layer of silicon dioxide, nominally 1.6 µm (± 0.1 µm) thick, is deposited on the topside of the silicon device layer, as illustrated in Fig. 1.3, by means of Plasma Enhanced Chemical Vapor Deposition (PECVD). This oxide layer will later serve as a releasable insulator material to provide electrical isolation as well as mechanical connection between portions of the single crystal silicon device structures.

The oxide layer is photolithographically patterned with the first level mask (**BRIDGE**), and subsequently etched by means of RIE. Figure 1.4 illustrates an exemplary structural pattern in the oxide layer after the photoresist is removed.

A second substrate is selected according to user's choice, as illustrated in Fig. 1.5. The baseline *a*MEMS™ process offers three selection choices – low-? silicon, high-? silicon, and Pyrex® 7740. The low-? silicon is a (100) oriented, Czochralski-grown (CZ), 100-mm silicon substrate with a nominal substrate resistivity between 0.1 O•cm and 20 O•cm. The high-? silicon is a (100) oriented, Float-Zone (FZ) grown, 100-mm silicon substrate with a nominal substrate resistivity of greater than 2000 O•cm. All substrate materials have a nominal thickness of 500 µm (± 10%).

Figure 1.4. Photolithography and RIE are used to transfer the pattern of the first level mask (BRIDGE) on to the oxide layer.

Figure 1.5. A second substrate is selected according to user's choice.

The front sides of the SOI wafer and the second substrate are adhesively bonded using a temperature ramping sequence up to 190 ºC, with a nominal bond line of 20 µm (± 5 µm), as illustrated in Fig. 1.6. The silicon substrate and the BOX layer of the SOI wafer are then removed, as illustrated in Fig. 1.7.

Figure 1.6. The front sides of the SOI wafer and the second substrate are adhesively bonded.

Figure 1.7. The silicon substrate and the BOX layer of the SOI wafer are removed.

A layer of evaporated aluminum is deposited on the silicon device layer with a nominal thickness of 0.5 µm (± 0.05 µm) to provide electrical contact to the silicon device layer. Photolithography and RIE are used to transfer the structural pattern of the second mask level (**STRUCTURE**) to the deposited aluminum layer, as illustrated in Fig. 1.8.

With the photoresist still intact, the structural pattern is further transferred into the silicon device layer by means of silicon DRIE. The photoresist is subsequently removed, as illustrated in Fig. 1.9.

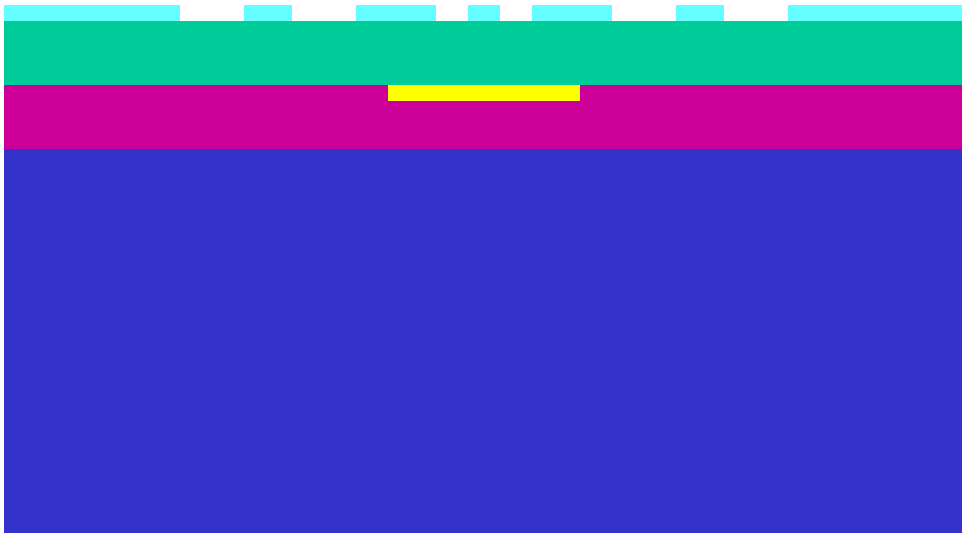


Figure 1.8. Photolithography and RIE are used to transfer the pattern of the second level mask (STRUCTURE) on to the aluminum layer. Note that photoresist is not shown in the figure.

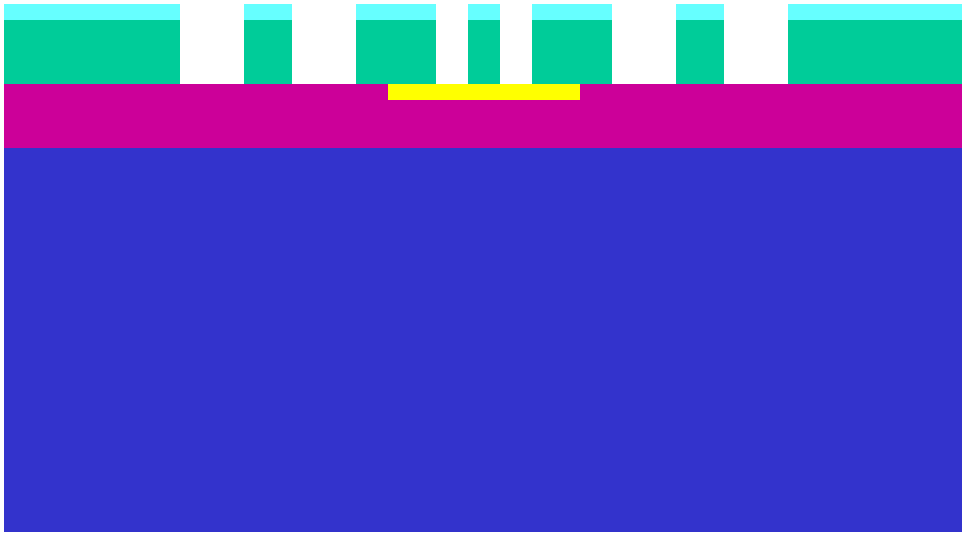


Figure 1.9. Silicon DRIE is employed to anisotropically transfer the structural pattern in to the silicon device layer.

The wafer is subsequently diced into chips or dies, which are then subjected to oxygen plasma to remove in part portions of the exposed adhesive bond to release the device structures, as illustrated in Fig. 1.10.

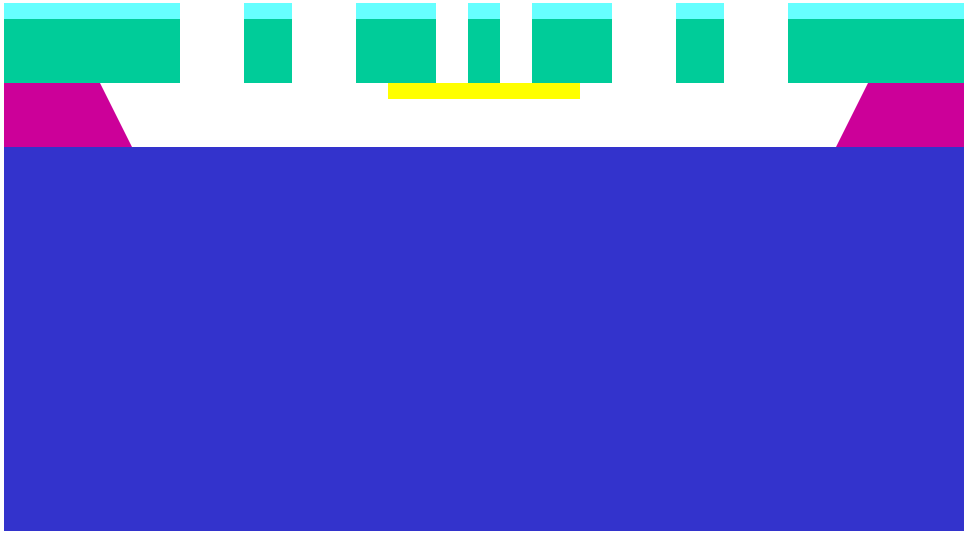


Figure 1.10. Oxygen plasma is used to dry release the devices.

1.3. Process Module Highlights

The *a*MEMS™ process incorporates a number of features that represent key elements in MEMS device implementation. The following are highlights of some selected process elements in detail.

PECVD Silicon Dioxide – A key feature described previously is the ability to incorporate dielectric structural elements for electrical isolation, as illustrated in Fig. 1.11. Defined in the BRIDGE mask, the PECVD oxide film is patterned using a CHF_3 and O_2 chemistry in a parallel-plate RIE system. Among other applications, the dielectric layer can be used to mechanically couple suspended silicon features, while effectively providing isolation against electrical breakdown, with devices demonstrated able to withstand greater than 1kV DC.

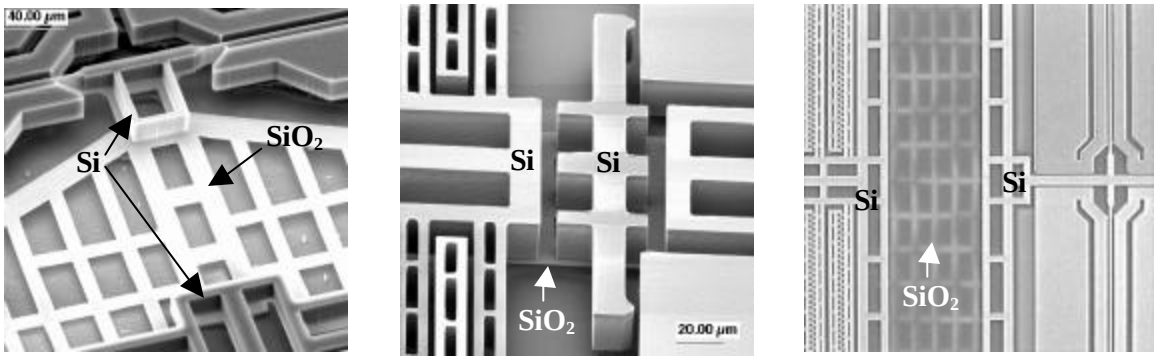


Figure 1.11. Exemplary designs illustrate the use of the PECVD silicon dioxide layer.

Aluminum Metallization – A second key feature is the chlorine-based aluminum RIE etching process, providing an anisotropic sidewall profile for fine-line aluminum metallization. This etching process maintains critical dimensions for further transferring to the silicon layer in a subsequent silicon DRIE processing step.

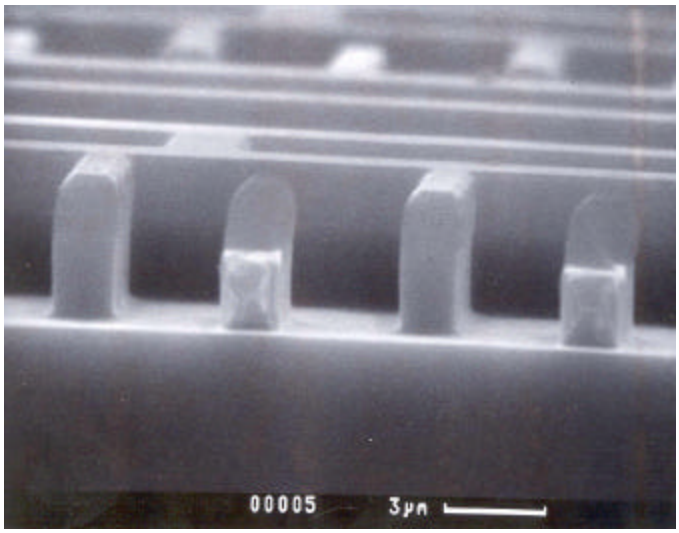


Figure 1.12. Chlorine-based RIE etching process provides anisotropic profile for fine-line aluminum metallization.

Silicon DRIE – Of particular note is the ability to exploit RSC's extensive capabilities in Si DRIE. While standard aMEMS processing typically has used 20um device layers, it may be easily extended to thicker layers. RSC has well-developed processes for thick layer etching, and has demonstrated aMEMS-based tunable capacitor devices with device layers of 80um, Fig. 1.13. This would provide one highly flexible element that may be customized in external access.

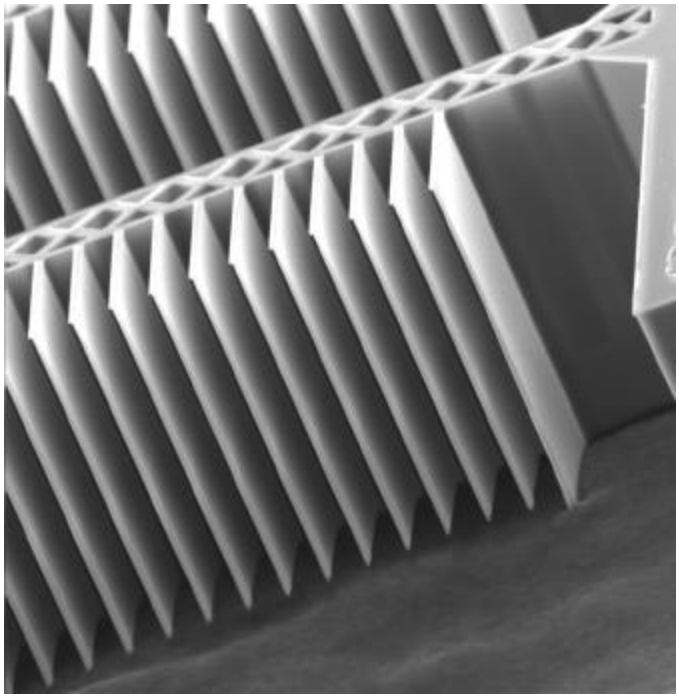


Figure 1.13. Silicon DRIE provides a feature.

Section 2

*a*MEMS™ Design Rules

2.1. Introduction

This section outlines the design rules dictated by the fundamental elements within the *a*MEMS™ process technology. The rules are a product of the accumulated and still-evolving process development and by experiences of the *a*MEMS™ technical staff, and reflect only the present status of the process technology. As the *a*MEMS™ process advances, the design rules may be revised from time to time to incorporate these improvements. It is our intention to have the revised design rules be backward compatible so that earlier versions of the design rules can still be accepted and used, although no guarantee is made nor implied.

The purpose of the design rules is to assist the users to better understand the fundamental elements, limitations, and unique features of the process technology. Therefore, it is to the users' best interest to comply with the rules, and not to stretch or "test the limits" of the rules, in order to ensure the greatest fabrication success possibility. In the cases where the boundaries set forth by the present design rules truly cannot satisfy your design needs, it is recommended that you discuss your special requirements with the *a*MEMS™ engineering staff prior to submission. It is our intention to accommodate your needs to the best of our capability as long as other users' work sharing the same run is not jeopardized.

Another uniqueness of the *a*MEMS™ process is its extreme versatility in material selections. To fully take advantage of this unique characteristic, we offer customized runs where the users would have more freedom in their MEMS designs by specifying, for example, an alternative device silicon thickness or a different substrate material. Please contact the *a*MEMS™ staff for further information with regards to accessing the customized runs.

2.2. Layer Name and Thickness

The baseline *a*MEMS™ process results the following layers as tabulated in Table 2.1 along with the nominal thickness.

Layer Name	Thickness (µm)	Pattern Definition	Comments
Aluminum	0.5	STRUCTURE	Blank metal on all silicon structures
Silicon	20	STRUCTURE	Structures defined in the silicon layer of SOI
Oxide	1.6	BRIDGE	Oxide layer patterned on the bottom side of the silicon layer
Bond Layer	20	STRUCTURE ∨ BRIDGE	Logical OR of the STRUCTURE and BRIDGE layers with a predefined amount of undercut
Substrate	500	N/A	Not patterned

Table 2.1. Layer names and thickness are tabulated along with pattern definitions.

2.3. Design Rules

Table 2.2 tabulates the basic design rules as well as the adopted naming scheme. This set of the basic rules is mandatory for all users to follow; and the naming scheme is used throughout this Design Handbook and will be used in any future communications between the users and the *a*MEMS™ engineering staff. It is highly recommended that the users adopt the same naming scheme to minimize any potential confusion.

Level Name	CIF Level Name	GDS Level Number	Min Feature (µm)	Min Space (µm)	Max Overlap (µm)	Min Anchor (µm x µm)	Max Released (µm)	Max Etched Area (%)
BRIDGE	BRDG	1	2	2	Unlimited	300 x 300	30	100
STRUCTURE	STRC	2	2 *	2	30	300 x 300	30	33
				4	Unlimited			

** When the 2-µm rule is used, the minimum unattached feature area must be 20 µm^2 or greater. Consequently, the smallest feature in STRUCTURE level is 2 µm by 10 µm.*

Table 2.2. Basic design rules are tabulated for the two masking levels in the *a*MEMS™ process.

2.3.1. BRIDGE Level

CIF level "BRDG" and GDS level "1" – The primary purpose for the BRIDGE level is to pattern a 1.6-µm PECVD oxide film. The critical dimension (CD) allowed in photolithography is 2 µm, and there are no other more stringent limiting factors in other processing steps such as the oxide etching process. And there are no limits in overlap distance between oxide features, nor in maximum area to be etched. The alignment specification to the STRUCTURE level is a minimum of 3 µm, although a 5-µm tolerance is highly recommended because the two-photolithography levels are conducted on the two sides of the silicon device layer.

2.3.2. STRUCTURE Level

CIF level "STRC" and GDS level "2" – The primary purpose of the STRUCTURE level is to pattern a 20-µm silicon device layer. The CD in photolithography is again 2 µm. When 2-µm gap spacing is used, the silicon DRIE further adds a requirement for open-ended features to have a maximum overlap distance not to be greater than 30 µm. Close-ended features must have a minimum gap spacing of 4 µm, and are not recommended for the 2-µm gap spacing. We also recommend a 33% maximum etched area to ensure optimal silicon DRIE etching uniformity. The alignment specification to the BRIDGE level is a minimum of 3 µm, although a 5-µm tolerance is highly recommended because the two-photolithography levels are conducted on the two sides of the silicon device layer.

2.3.3. Anchoring and Releasable Features

The structure releasing process is a dry process by means of oxygen plasma removing portions of the exposed adhesive bond layer. It is a timed etching process set to guarantee that all continuous features 30 µm or smaller are released, and that all continuous features 300 µm or larger are not fully released or are anchored. It is highly recommended that features between 30 µm and 300 µm not to be used in the baseline *a*MEMS™ process runs as there will be no guarantee whether these features will be released or anchored. Should a user require a different specification for the released versus non-released dimensions, a customized run is recommended as the releasing specification can be indeed modified to a certain degree.

2.4. Pattern Polarity and Other Mask / Layout Related Criteria

Both BRIDGE and STRUCTURE levels should be clear field, resulting in drawn patterns being opaque on the masks, and features on the wafer. In other words, the users should keep in mind to draw patterns that are intended to form features on the wafer.

Non-rectangular polygons (a.k.a. non-Manhattan geometries) are acceptable geometries in the mask rendering process. The users should feel free to use this capability and include arcs and polygons as needed.

Self-intersecting polygons as exemplarily illustrated in Fig. 2.1 (a) are illegal geometries; and it is the user's responsibility to correct them before submission. A common cause for the illegal geometry is a drawing error where the true geometry may be as illustrated in Fig. 2.1 (b). If the user must have the "illegal-geometry" pattern as illustrated in Fig. 2.1 (a), a multiple-polygon method can be used to simply replace the self-intersecting polygon by a plural of non-self-intersecting polygons, as illustrated in Fig. 2.1 (c).

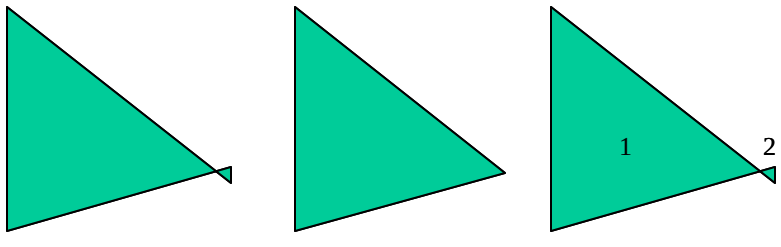


Figure 2.1. An illustration shows (a) an illegal self-intersecting polygon geometry, (b) a common correction to the illegal polygon, and (c) a multiple-polygon method of correction should the polygon pattern in (b) is truly what the user designs.

2.5. Material and Process Geometry Specifications

Material and process geometry specifications outlined in this section are to be used as references only, and are not guaranteed.

Lithography – Photolithography is maintained to within ±0.1 µm per side of the original art work.

Aluminum – 0.5 µm e-beam evaporated thin film aluminum. This aluminum layer is dry etched in a chlorine-based chemistry using the STRUCTURE pattern mask. The same photoresist pattern is subsequently used for the silicon DRIE. Consequently, aluminum is present on all silicon features in the final *a*MEMS™ devices. The aluminum dry etch is aimed to be an anisotropic process, with an anticipated maximum undercut no greater than 0.2 µm per side. Some further details of this process can be observed in Fig. 1.12. Thickness variation is controlled to within ±10 %.

Silicon – 20 µm single crystal SOI device layer silicon. This silicon layer is patterned using the STRUCTURE pattern mask in a DRIE process. The sidewall profile of the silicon structures contains the typical features of the Bosch DRIE process, such as "scallop." The maximum amount of undercut is controlled to no greater than 0.2 µm per side. The residual stress within the silicon layer depends on the substrate used. Table 2.3 outlines the silicon residual stress on three commonly used substrates at room temperature. Thickness variation is expected to be within ±1 µm.

Substrate Used	CTE (10^{-6} / °C)	Silicon Residual Stress (MPa) at Room Temperature	
		Nominal	Typical Range
Silicon	2.3	10	0 to 30
Pyrex	3.2	-40	-20 to -60
Vycor	0.7	60	30 to 80

Table 2.3. Silicon residual stress levels on three commonly used substrates at room temperature.

Dielectric Layer – 1.6 µm PECVD silicon dioxide. The silicon dioxide film is patterned using the BRIDGE pattern mask in a fluorine-based (CHF_3) RIE chemistry, which is expected to produce minimal undercut. The residual stress within the silicon dioxide film when deposited on a silicon substrate is nominally -30 MPa, with a typical range from -15 MPa to -50 MPa. The stress level changes slightly when different substrate material is used. Thickness variation is controlled to within ±10 %.

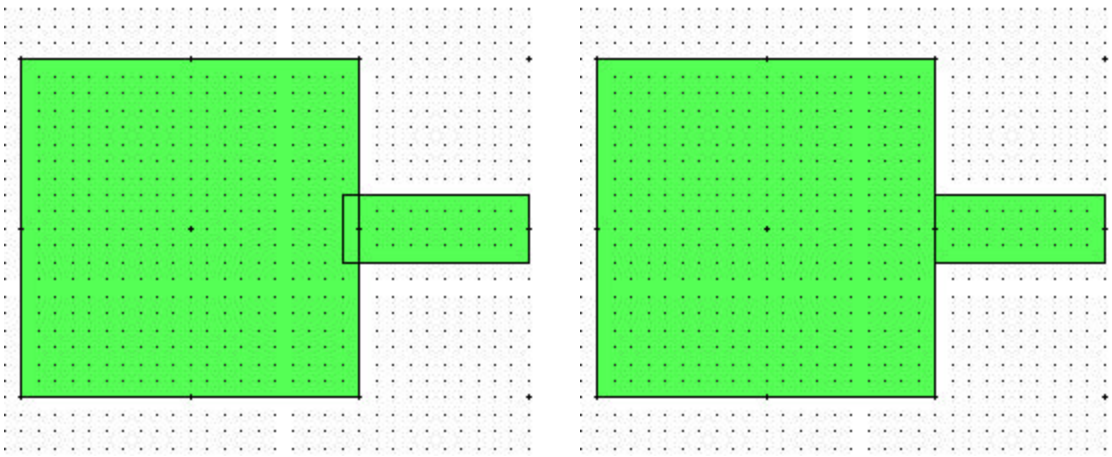
Bond Layer – 20 µm cured epoxy. The bond layer is masked by both the remaining silicon and silicon dioxide film, and is etched in oxygen plasma, which produces a controlled amount of undercut. The oxygen etch is designed to completely undercut and therefore release structures that are 30 µm or narrower in width, and not to fully undercut (therefore leaving intact) structures that are 100 µm or wider in width. For the purpose of mechanical integrity, it is recommended that any designed anchoring structures having a minimum width of 300 µm. Thickness variation is expected to be within ±5 µm.

Substrate – Substrate is not etched or patterned.

2.6. Design Recommendations

It is highly recommended that the users remain within the boundaries of the design rules at all time. When a run is shared among users, designs failed to follow the design rules will be rejected to ensure that other users' designs sharing the same run are not jeopardized.

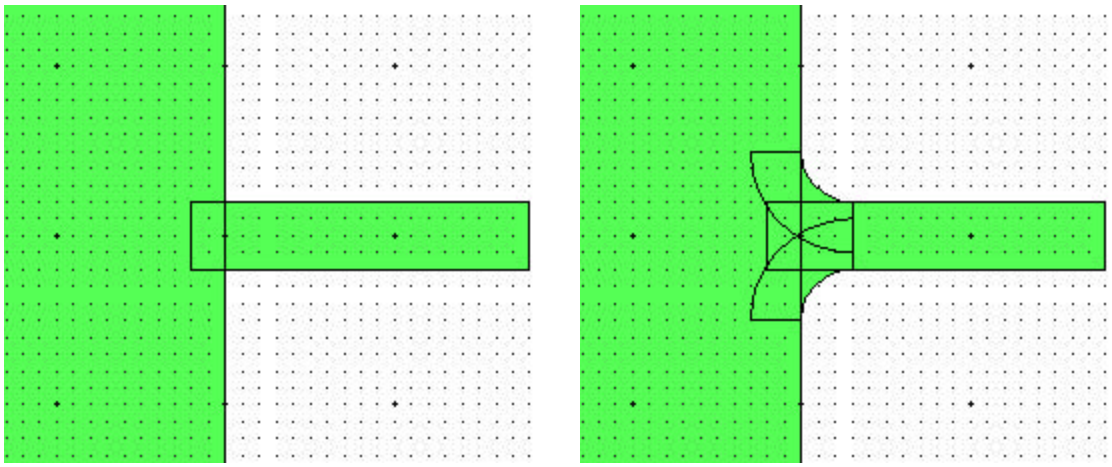
Overlapping Adjoining Features in Drawing – It is always a good practice to have certain overlap (e.g., 1 µm) between adjoining features in layout. This is to ensure that the features will be digitized correctly to form a single joined element. Figure 2.2 below illustrates graphically this recommendation.



(a) Overlap is recommended in layout. (b) Chance for resulting separate features.

Figure 2.2. Overlap between adjoining features is recommended to ensure correct digitization.

Minimizing Stress Points – Concentrated stress points in a suspended feature are one of the leading causes for structural breakage. They should be minimized or avoided if possible. Figure 2.3 below illustrates graphically this recommendation.

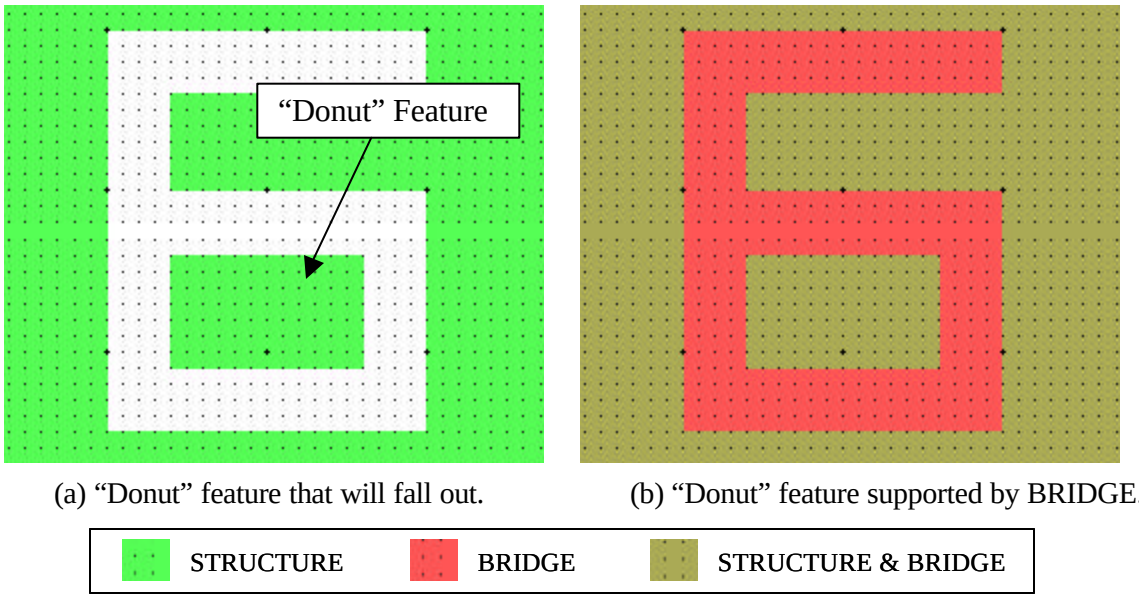


(a) Uncompensated stress point at anchor. (b) Recommended design if possible.

Figure 2.3. Concentrated stress points such as illustrated in (a) should be replaced with recommended designs such as the one illustrated in (b).

Handling "Donut" Features – "Donut" features refer to structures with an unattached small island that would be fully released in the oxygen-plasma releasing step. These "donut" features must be

avoided, as they would fall out and result in debris / yield problem after release. A common place where these "donut" features appear is in generating numbers and alphabet letters. One acceptable solution for having "donut" features in the STRUCTURE layer is to use the BRIDGE layer for support. Figure 2.4 below illustrates graphically this solution.



(a) "Donut" feature that will fall out. (b) "Donut" feature supported by BRIDGE.

Figure 2.4. The "donut" feature in the STRUCTURE layer in (a) (unacceptable) is supported by the BRIDGE layer in (b) (acceptable).

Residual Stress and Stress Gradient – Residual stress within each thin film should be taken into consideration when designing MEMS devices. Tensile-stressed material may crack, while compressive-stressed material may buckle. Structural dimensions should be carefully evaluated while considering these residual stress issues. In designs where multiple films with different CTE are stacked on top of one another, stress gradient may cause the composite structure to deflect out of plane. It is highly recommended to take these stress properties into consideration in one's designs.

2.7. Layout Requirements and Submission

Each chip site is 6,350 µm x 6,000 µm. A restricted space of 150 µm wide along all four edges of the chip is reserved for chip dicing purpose. It is highly recommended that the users allow 200 µm dicing space instead, and leaving a design area of 5,950 µm x 5,600 µm. It is also recommended that the users center their data to minimize any potential confusion, and have a design area of X (-2975, +2975) in µm and Y (-2800, +2800) in µm (see Figure 2.5).

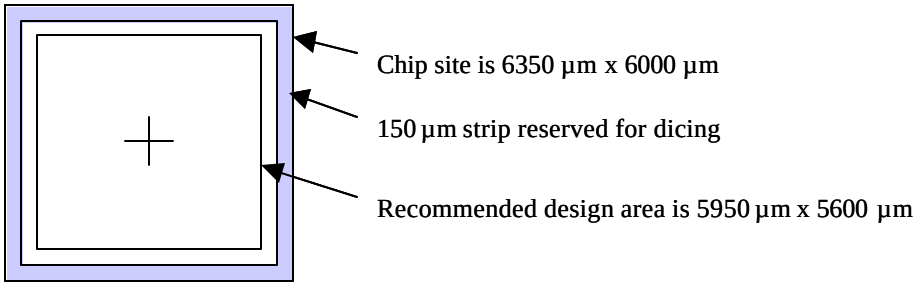


Figure 2.5. Recommended design area.

Cell names should consist of only the 26 standard characters (capital "A-Z" or lower case "a-z"), the numeral numbers "0-9", and the underscore character "_".

Custom fabrication run can have a chip size of 6,350 µm x 6,000 µm, 6,350 µm x 12,000 µm, 12,700 µm x 6,000 µm, or 12,700 µm x 12,000 µm. Custom fabrication run can also specify a substrate choice of low resistivity silicon (=20O·cm), high resistivity silicon (=2000O·cm), Pyrex, or Vycor glass, while multi-user fabrication runs use a standard substrate material of high resistivity silicon (=2000O·cm).

Designs may be submitted in GDSII format. Please contact us via email at jyao@rwsc.com for other possible format options and / or for further information. Users must also complete an *a*MEMS submission form along with the submission of the electronic data file.

References

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Appendix 1: aMEMS™ Example Devices

The *a*MEMS process offers unparalleled flexibility and utility for MEMS device implementation. The ability to fabricate a large number of different device types in this process offers the potential for increased fabrication volumes, benefiting cost and process control. A broad range of device types have been demonstrated in a single *a*MEMS fabrication run, further illustrating the flexibility of the process and the range of potential applications the technology can support.

General Information About the Application Examples Fabrication Run

Table A1. General Information – Application Examples Fabrication Run

Fabrication Run Start Date	January 7, 2005	
Fabrication Run End Date	February 23, 2005	
Number of Wafers	6	
Number of Test Wafers	10	
Wafer Specs		
SOI Device Layer Thickness	20	µm
Resistivity	0.01 – 0.02	Ω•cm
SOI BOX Layer Thickness	1.0	µm

Application Examples Demonstration Structures

Table A2. List of application examples demonstration structures

#	Name	Intended Functionality
1	TunableCap4	Tunable capacitor with capacitance increasing w/ increasing tuning V
2	TunableCap4R	Tunable capacitor with capacitance decreasing w/ increasing tuning V
3	Beta_LatchNRelease	Demonstrating mechanical latching and releasing mechanism
4	VPlate	Large parallel plate structure offering vertical movement
5	Accel1,2,3,4	4 Accelerometers with resonant frequencies of 150, 300, 450, 830Hz
6	CombRes	Resonant devices for resonator and filter applications
7	Shaped	Shaped electrode devices
8	ShapedContact	Shaped electrode devices with side-wall contact
9	5B400A	Current sensor with high voltage isolation

Results

The information presented in this section contains average test results of a limited sample size, intended to provide an informative description of the application examples of the *a*MEMS process technology. All example devices documented here were fabricated in a single fabrication run (R2).

Tunable Capacitors

Capacitor banks were formed using silicon DRIE to create comb structures with a finger width and spacing nominally 2µm, and a height of 20µm. A tunable capacitor (Fig. A2) consists of a tuning and an RF capacitor bank, supported by silicon flexures of a designed rigidity. Further design details can be found in Refs. [1,3,5]. When a voltage is applied to the tuning capacitor bank, the electrostatic attracting force moves the entire structure, and subsequently changes the capacitance of the RF capacitor bank, which can be configured to result, in response to the applied tuning voltage, either an increase ("positive" tuning, Fig. A3a) or a decrease ("negative" tuning, Fig. A3b) in its capacitance value.

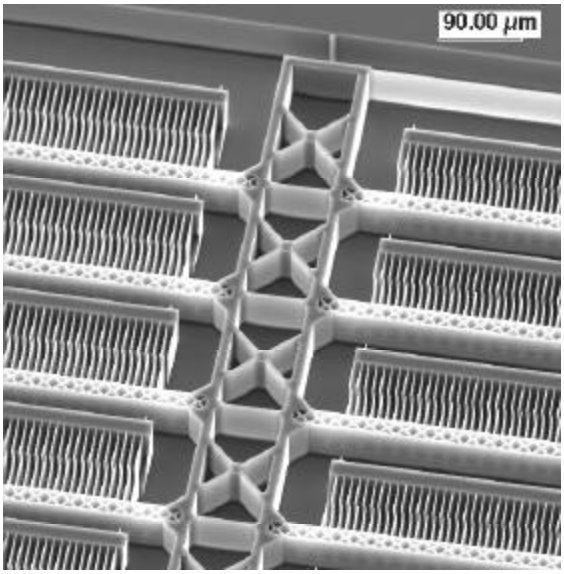
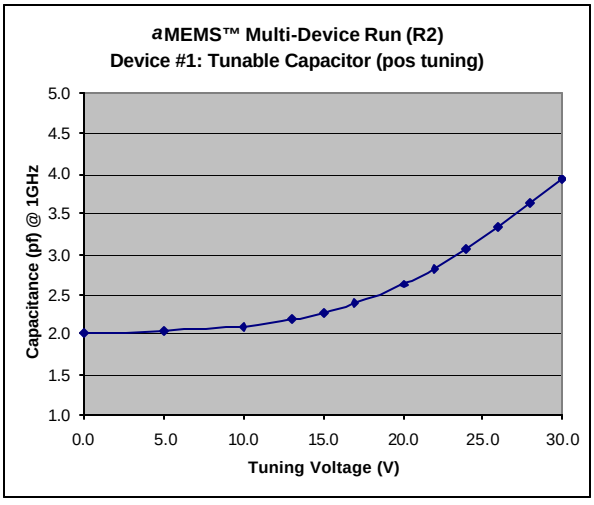
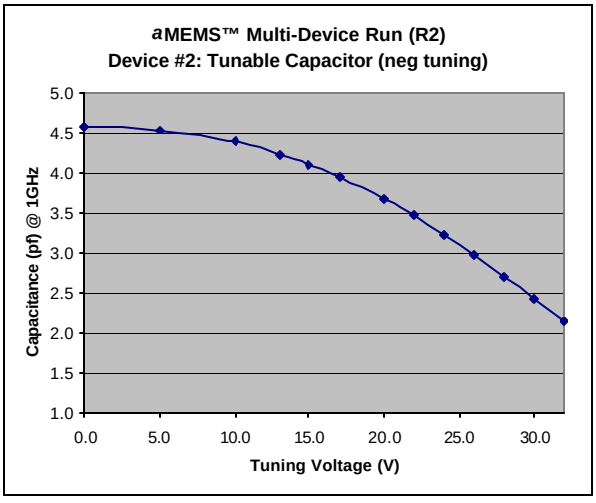


Figure A2. SEM image of a tunable capacitor



(a)

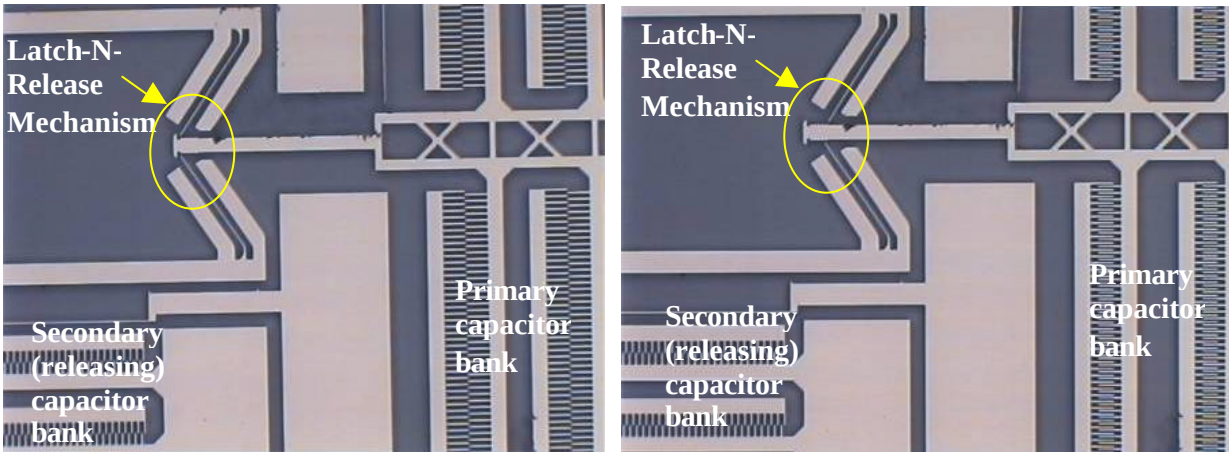


(b)

Figure A3. Capacitance value at 1 GHz is plotted against the applied tuning voltage for (a) a positive and (b) a negative tuning capacitor.

Mechanical Latch / Release Mechanism

Mechanical latching and releasing mechanisms have a broad range of applications in re-configurable systems, safing and arming, and mechanical information storage. The device (Fig. A4) consists of a primary capacitor bank holding a mechanical latching mechanism, which can be released by a second set of capacitor bank. The required electrostatic voltage for the capacitive actuators is at a low value of less than 12V. The latching and releasing mechanisms have been demonstrated in the form of capacitance change of the primary capacitor bank. Figure A5 is a plot of the measured capacitance values at various un-latched and latched positions. The build-in releasing mechanism enables the device to be re-configurable, with the use of a second bank of capacitors.



(a) (b)

Figure A4. The latching and releasing device is shown (a) in its un-latched and un-biased position, and (b) when latched in its forth of the total five latching positions.

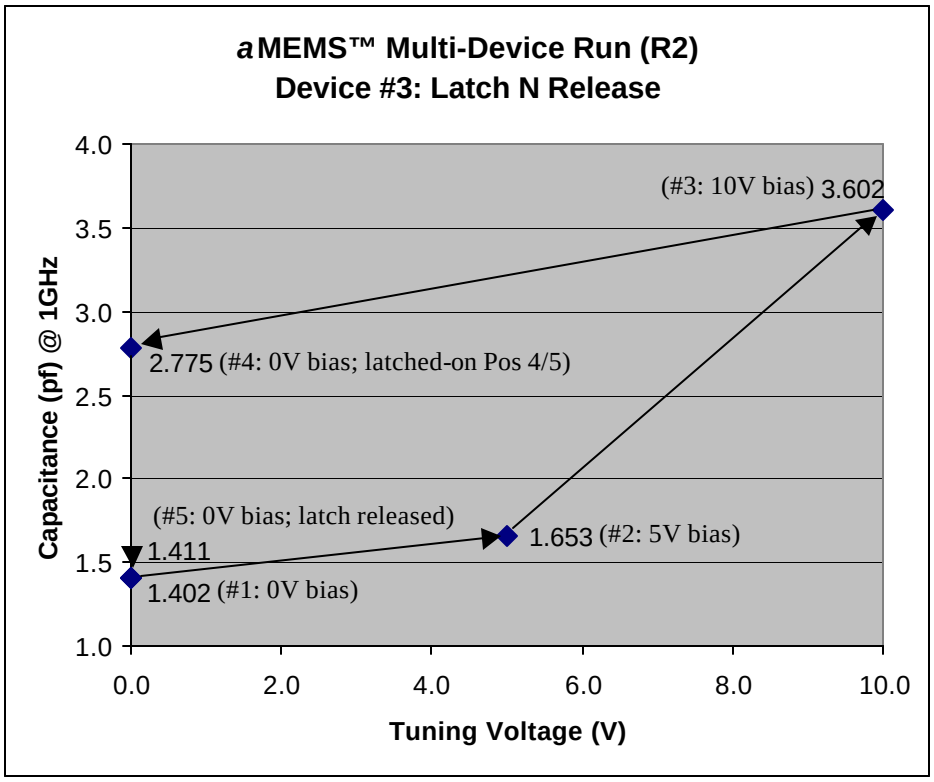


Figure A5. The Latch-N-Release device is demonstrated in terms of its capacitance change.

Parallel Plate Structure with Vertical Movement

Although the majority of the application examples demonstrated using the *a*MEMS™ process technology, vertical (out-of-plane) movement can also be produced. The particular example demonstrated here is controlled by means of electrostatic actuation. The device (Fig. A6) consists of a large planar plate (1650µm by 1520µm) suspended by flexures to be in parallel with the underlying substrate. When a voltage is applied between the plate and the substrate, the electrostatic attracting force displaces the mirror plate.